MODELLING AND SIMULATION OF MULTI-SAMPLING DEADBEAT CURRENT CONTROLLER WITH TIME-DELAY COMPENSATION FOR GRID-CONNECTED INVERTER

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DEDICATION

I dedicate this work to my beloved parents, my beloved wife, and children.

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ABSTRACT

Digital controller realisations suffer from a phase lag induced by time delay. This phase lag makes it hard for inverter controller to maintain stability and robustness, especially during grid-impedance perturbations. This research aims at mitigating the inherent one-sampling-period delay associated with deadbeat current control without requiring an anti-aliasing filter. First, a deadbeat current controller was modelled with the right tuning polynomial and with the caution of not cancelling the poles and zeroes to improve the performance of the system, as well as its resilience against parameter variation. The designed controllers were tested using Nyquist and Bode plots, and their responses were acceptable with the control margin stability. In the second part, time delay condition has been added to the model to mimic the real delay and a quadruple-sampling deadbeat current controller was modelled, which reduced the one-sampling-period delay of the traditional deadbeat current controller to $\frac{1}{4}$ sampling period. This time-delay mitigation improved the bandwidth of the controller, as well as reduced the total harmonics injected into the grid. In the last part, a comparison between the performances of the proposed quadruple-sampling deadbeat current controller and the conventional proportional-integral controller was intuitively carried out using the same simulation setup. The proposed method achieved an improvement of 120 μs from that of the Proportional Integral (PI) current controller. In terms of Total Harmonic Distortion (THD), the quadruple-sampling design method exhibited 1.01% in THD current and 0.12% in THD voltage as compared to the PI controller with 4.03% and 0.18% in current and voltage THDs, respectively. Finally, the two controllers were compare subjected to grid parameter variation of 40% and 80% and from the results obtained, the quadruple-sampling design method displayed good current tracking, improve time-delay compensation, and robustness against parameter variation.

ABSTRAK

Realisasi pengawal digital mengalami ketinggalan fasa yang disebabkan oleh kelewatan masa digital. Selang fasa ini menyukarkan pengawal penyongsang untuk mengekalkan kestabilan dan keteguhan, terutamanya semasa gangguan pada talian impedan grid. Projek ini bertujuan untuk mengurangkan kelewatan tempoh satu persampelan yang dikaitkan dengan kawalan arus kematian denyut tanpa memerlukan penapis anti-aliasing. Pertama, pengawal arus kematian denyut dimodelkan dengan polinomial penalaan yang betul dan dengan berhati-hati untuk tidak membatalkan kutub dan sifar untuk meningkatkan prestasi system penukar grid, serta daya tahannya terhadap variasi parameter. Pengawal yang direka telah diuji menggunakan plot Nyquist dan Bode, dan respons mereka adalah didalam julat pengawalan stabili. Dalam bahagian kedua, keadaan kelewatan masa telah ditambahkan pada model untuk meniru kelewatan sebenar dan pengawal arus kematian denyut bagi pensampelan empat kali ganda telah dimodelkan, yang mengurangkan kelewatan tempoh satu persampelan pengawal arus kematian denyut tradisional kepada 1/4 pensampelan tempoh. Pengurangan kelewatan masa ini akan meningkatkan lebar jalur pengawal, serta jumlah harmonik yang disuntik ke dalam elektrik grid. Pada bahagian terakhir, perbandingan antara prestasi pengawal arus kematian denyut pensampelan empat kali yang dicadangkan dan pengawal kamiran berkadar (PI) konvensional telah dijalankan secara intuitif menggunakan persediaan simulasi yang sama. Kaedah yang dicadangkan mencapai peningkatan 120 μs daripada pengawal arus PI. Dari segi jumlah herotan harmonik (THD), kaedah reka bentuk pensampelan empat kali ganda menunjukkan 1.01% dalam THD arus semasa dan 0.12% dalam THD voltan berbanding dengan pengawal PI dengan 4.03% dan 0.18% dalam THD semasa dan voltan, masing-masing. Akhirnya, kedua-dua pengawal dibandingkan tertakluk kepada variasi parameter grid sebanyak 40% dan 80% dan daripada keputusan yang diperoleh, kaedah reka bentuk pensampelan empat kali ganda memaparkan

pengesanan arus yang baik, pampasan kelewatan masa yang luar biasa, dan keteguhan terhadap variasi parameter.

CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

P_m	–	Phase margin
W_{pc}	–	Phase cross-over frequency
W_{gc}	–	Gain cross-over frequency
f_s	–	Switching frequency
f_{sw}	–	Sampling frequency
U_{dc}	–	DC-link voltage
L_{gs}	–	Grid impedance
L_i	–	Inverter-side inductor
L_g	–	Grid-side inductor
U_g	–	Grid nominal voltage
C_f	–	Filter capacitance
k_d	–	Damping factor of capacitor current
ζ	–	Damping ratio
T_S	–	Sampling period
${A_{(z)}}^+$ and ${B_{(z)}}^+$	–	Poles and zeros inside unit circle
${A_{(z)}}^-$ and ${B_{(z)}}^-$	–	Poles and zeros outside unit circle
z^{-d}	–	Inherent delay in plant
K_{pwm}	–	Gain of full-bridge three-phase inverter
$I_d I_{q_{ref}}$	–	Direct-quadrature reference current
$I_d I_{q_M}$	–	Measured direct-quadrature current
$U_{V_{1_{abc}}}$	–	Control voltage
$U_{V_{2_{abc}}}$	–	Feed-forward voltage
V_{Dc_M}	–	Measured DC voltage
$V_{Dc_{Ref}}$	–	Reference DC voltage

$U_{V_{PCC}}$	–	Feed-forward voltage from point of common coupling
m_s	–	Single-update PWM wave
V_{iabc}	–	Inverter-side three-phase voltage
V_{cabc}	–	Capacitor-side three-phase voltage
V_{gabc}	–	Grid-side three-phase voltage
f_r	–	Resonance frequency
f_s	–	State-variable sampling frequency
T_d	–	Maximum time delay
$f_{critical}$	–	Critical frequency
P	–	Active power
Q	–	Reactive power
DG	–	Distributed generation
GCI	–	Grid-connected inverter
MG	–	Microgrid
LCL	–	Inductor-capacitor-inductor
VSI	–	Voltage-source inverter
MB	–	Model-based
MF	–	Model-free
SP	–	Smith predictor
MSP	–	Modified Smith predictor
DBC	–	Deadbeat controller
MPC	–	Model predictive controller
DT	–	Damping techniques
FBT	–	Filter-based techniques
SSI	–	Shifting sampling instant
FPGA	–	Field-programmable gate array
DPWM	–	Digital pulse-width modulation
L	–	Inductor
LC	–	Inductor-capacitor
PI	–	Proportional-integral
N/A	–	Not applicable
I	–	Current

V	–	Voltage
SL	–	Single loop
DL	–	Double loop
DSDU	–	Double-sampling double-updating technique
QSQU	–	Quadruple-sampling quadruple-updating technique
MSMU	–	Multi-sampling multi-updating technique
ICF	–	Inverter-side current feedback
GCF	–	Grid-side current feedback
CCF	–	Capacitor current feedback
SOGI	–	Second-order generalised integrators
QRCT	–	Quasi-resonant component technique
ESRT	–	Extending stable region technique
GVFF	–	Grid voltage feed-forward
CVFF	–	Capacitor voltage feed-forward
PR	–	Proportional-resonant
SLDAT	–	Single-loop delay addition techniques
SLDT	–	Single-loop damping techniques
SO	–	State observer
QPI	–	Quasi-proportional-integral
WFP	–	Weighted filter predictor
SSITUT	–	Shifting sampling instant toward PWM update time
UIAC	–	Update immediately after calculation finished
TCS	–	Triangular carrier signal
PCCs	–	Predictive current controllers
Ή∞	–	H-infinity
LPF	–	Low-pass filter
DSPs	–	Digital signal processors
LP	–	Linear predictor
ANN	–	Artificial neural network
TNE	–	Techniques not explicit
NCO	–	Natural current observer

THD	–	Total harmonic distortion
GCV	–	Grid current variation
FIV	–	Filter inductance variation
GVV	–	Grid voltage variation
PV	–	Power variation
GIV	–	Grid impedance variation
MM	–	Model mismatch
DBCC	–	Deadbeat current control
IIV	–	Inverter-side inductance variation
LIV	–	Load inductance variation
LRV	–	Load resistant variation
FCV	–	Filter capacitance variation
BEMF	–	Back EMF
PRCV	–	Phase reference current variation
ARCV	–	Amplitude reference current variation
GSC	–	Grid short circuit
HIC	–	High inrush current
PJ	–	Phase jump
PE	–	Power error
PAS	–	Power angular shift
PZCA	–	Pole-zero cancellation approach
FRA	–	Factorisation approach
SVDA	–	State-variable derivation approach
HBDA	–	Hybrid design approach
RCA	–	Robust control approach
ODA	–	Other DBC design approaches
SVPWM	–	Space vector pulse-width modulation
QSSVDDCC	–	Quadruple-sampling state-variable-derivative deadbeat current controller

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Research background

The majority of the world's existing energy needs are met by conventional forms of energy. There are scarce reserves of these resources on earth. Factors such as pollution, CO_2 emissions, and global warming degrade the environment. Consequently, renewable energy sources are increasingly becoming popular in the modern world. Among all renewable power sources, solar energy receives the most attention as the best replacement for conventional energy due to the source's accessibility. Technical advancements in solar energy systems make their implementation viable in a variety of applications.

Inverters are a major element of a photovoltaic (PV) system connected to the electrical grid. It changes DC energy generated by solar panels into grid-compatible AC power. In terms of architecture, the three primary inverter topologies are the central inverter, string/multi-string inverter, and module-integrated microinverter [1]. Topologies with a centralised inverter are typically chosen for large-scale power generation, since they have a common maximum power point tracking (MPPT) and a centralised inverter connected to PV arrays (series-parallel connection of PV modules). The string inverter topology is a scaled-down variant of the central inverter architecture, in which a certain number of modules are connected in series (string), and the inverter that is attached to that string is referred to as the string inverter [2], [3]. In this topology, each string has its own MPPT. The multi-string topology is an evolution of the string inverter design for larger systems. In this design, each string is equipped with its own DC-DC converter, and all of the strings are connected to a single inverter.

Lastly, there is the module-integrated microinverter, in which each PV module is equipped with its own inverter and an individual MPPT [4], [5]. All these inverter topologies can take current or voltage as input; when current is used, the inverter is referred to as a current-source inverter, and when voltage is used, it is referred to as a voltage-source inverter.

In grid-connected inverter applications, traditional controllers are primarily proportional-integral-derivative (PID) and hysteresis controllers[6]. PID controllers are used to control the inverter's output voltage and frequency to match the grid voltage and frequency. The controller continuously changes the inverter output based on the difference between the desired and actual output [7]. Hysteresis controllers move between two voltage levels to adjust the output voltage of an inverter. A hysteresis band, which is a range of values specified by an upper and lower limit, is used to flip between the two levels [8]. When the grid voltage passes the upper or lower limit of the hysteresis band, the controller switches the inverter output between the two voltage levels. Because of their simplicity and resilience, both of these controllers have been frequently employed in grid-connected inverter applications [9]. More advanced control methods, such as model predictive control (MPC) and sliding mode control (SMC), and deadbeat control have been developed and are being employed in some applications to improve performance and efficiency of the inverter connected to the grid.

Deadbeat current control is one of the modern control methods used in grid-connected inverters to accurately control the output current waveform [10]. The goal of deadbeat current control is to achieve fast dynamic response and zero steady-state error. In a grid-connected inverter system, the inverter is required to inject a sinusoidal current into the grid that is in phase with the grid voltage. Deadbeat current control is used to ensure that the current injected by the inverter matches the desired waveform as closely as possible, even in the presence of disturbances such as changes in the load [11]. Deadbeat current control is typically implemented using a linear state-space model of the inverter and grid. The controller uses this model to calculate the control inputs required to achieve the desired current waveform. The controller continuously updates the control inputs to track changes in the grid and load conditions [11]. One of the main advantages of deadbeat current control is its fast response time, which helps to minimize the harmonic distortion of the current waveform [12]. Additionally, the zero steady-state error achieved by the controller ensures that the current waveform is accurately maintained even under changing conditions [13]. Deadbeat current control has been widely used in grid-connected inverter applications for its robustness and accuracy. However, it requires a precise model of the inverter and grid, which can be challenging to obtain in some cases. Additionally, the controller can be sensitive to modelling errors and associated one sampling period delay [14], which can limit its performance in some applications.

High-performance control systems for power electronic inverters are now most often implemented digitally. This is brought about by the ease of use and flexibility of digital controllers, the inclusion of safety and monitoring features, and the steadily declining cost of digital control platforms [15]. However, digital implementation has some drawbacks, with the most challenging being the digital time delay [16].

Time delay refers to the period of time taken for a system to respond to a change or input [17]. In various fields, including engineering, control systems, and signal processing, time delay is a phenomenon that occurs when there is a noticeable gap between the application of a stimulus or signal and the system's corresponding response [18].. In a dynamic system, such as an inverter plant, time delay can arise due to several factors, including processing and communication delays. Processing delays occur when there is a delay in the system's ability to process information or execute control actions. Communication delays occur when there is a time lag in transmitting signals between different components or subsystems of the plant. Time delays can have significant implications for the stability, performance, and overall behaviour of a system. They can lead to oscillations, instability, and even system failure if not properly accounted for in the design and control processes. Therefore, understanding and managing time delays is crucial in ensuring the reliable and efficient operation of complex systems, such as inverter system.[19]. Compensators are used in an effort to lessen or do away with the delays caused. Time-delay mitigation methods can be classified in terms of sensitivity to the modelling of the system. Model-based methods have a higher degree of precision but their precision is highly reliant on the accuracy of system modelling, while model-free methods have a lower degree of precision but are not affected by the correctness of the model. Among prominent controllers from the model-based delay compensation approach are the deadbeat controller (DBC) and the model predictive controller (MPC). On the other hand, prominent methods from the model-free approach are the filter-based technique (FBT) and the technique of shifting the sampling instants (SSI) of the control variable [17].

The control of grid-connected inverters is classified into primary, secondary and tertiary controls. In this research work, the focus was strictly on the improvement of the primary control. In grid-connected inverters, primary control can be implemented in either analogue or digital form, where analogue control involves the manual tuning of traditional controllers, such as the proportional-integral (PI), proportional-integral-derivative (PID), or proportional-resonant (PR) controllers, while digital control involves the use of micro-controller to implement the control design, such as the deadbeat control, the model predictive control, etc. Deadbeat control refers to a condition in which the response is exactly the same as the reference input after a defined and finite time interval, but only at sampling instants. This type of control design is carried out in a discrete form. For decades, the deadbeat controller has gotten a lot of attention because of its benefits, which include zero steady-state error [11], [20], [21], straightforward implementation on a digital control system, low current harmonics, fast dynamic response [22], and time-delay compensation capabilities [10], [17], [23]. However, this type of controller has been criticised for its aggressiveness, its sensitivity to model accuracy, and the existence of the inherent one-sampling-period delay. But these issues can be minimised by using a tuning polynomial, among others. In [10], the modelling of the controller used time-delay consideration and model-free time-delay compensation.

1.2 Problem statement

Digital signal processing improvements allow inverters to be controlled by a microprocessor. Digital control is more reliable and flexible than analogue control and it is also programmable. The most technically problematic downside of digital control implementation is the phase lag caused by sampling and updating control quantities, calculations in the digital signal processor, and the sampling and holding of the digital pulse-width modulator. This phase lag challenges the controller’s resilience.

Deadbeat current control (DBCC) has been criticised for it aggressiveness to control actions, sensitivity to model accuracy, and inherent one-sampling-period delay. These drawbacks reduce the potential of this controller to achieve fast current tracking and resilience to disturbances. In the literature, a state observer has been used to lessen the sensitivity to model accuracy and the method of shifting sampling and updating instants has been used to mitigate the time delay associated with this type of controller. However, among the techniques of shifting sampling and updating instants for time-delay mitigation, the single-sampling single-updating (SS-SU) and the double-sampling double-updating (DS-DU) methods are associated with one-period time delay and half-period time delay, respectively, and may be susceptible to noise-related issues [24]–[27].

Furthermore, there is a need to further reduce this residual time delay to significantly enhance the achievable dynamic response of the controller [28], [29]. The multi-sampling multi-updating method can reduce the residual delay by some fraction compared with those of SS-SU and DS-DU, but this method introduces some nonlinearities, mainly because of the discontinuity of the modulating waveform [15]. Therefore, the MS-MU method relies on the use of an anti-aliasing filter in the feedback path [30], [31] However, the added filter compromises the dynamic benefits obtained by the MS-MU method [26], [29], [32]–[37]. Hence, this research work introduced novel approaches to enhance the accuracy and efficiency of the DSDU method. One key aspect involved the modelling of time-delay terms, which aimed to reduce sensitivity to the accuracy of the model. Additionally, the study proposed the utilization of the quadruple-sampling method to further minimize the residual time delay by half. By doing so, it eliminated the necessity for an anti-aliasing filter commonly employed in MSMU. Overall, these innovations not only improved the DSDU method but also eliminated the need for an additional component, leading to enhanced performance and efficiency.

1.3 Aim

This research aimed at mitigating the inherent one-sampling delay associated with deadbeat current control without requiring an anti-aliasing filter.

1.4 Objectives

This research work embarked on the following objectives:

1. To develop a deadbeat current controller in order to improve the voltage and current performance of a grid-connected inverter.

2. To model and simulate a quadruple-sampling deadbeat current controller to minimise the one-sampling-period delay inherent in a deadbeat controller for grid-connected inverter application.
3. To compare the performance improvement between the proposed quadruple-sampling deadbeat current controller with the performance of the conventional PI-based current controller

1.5 Scope of research

The limits of the research work are as follows:

1. A three-phase full-bridge grid-connected inverter with a power rating of 80 kW was used.
2. A 680V DC source was applied to the inverter.
3. The AC nominal voltage used in this simulation was 230 V.
4. Two resistive-inductive loads of 15 kW, 2 kvar and 20 kW, 3 var were used.
5. Quadruple-sampling deadbeat current control was used for the inner loop and PI voltage control was used for the outer loop.
6. MATLAB/Simulink 2021a was used as a tool to test and compare the performance of the controllers.
7. A grid-impedance variation from 15.6 µH to 21.6 µH was used to test the stability of the controllers. This was because grid impedance varies as a result of other inverters connected to the grid, which may result in a variable resonance frequency that challenges the stability and robustness of the LCL filter of an inverter.

1.6 Contribution of the research

The main innovation of this study involves integrating two notable strategies for time delay compensation: the quadruple-sampling technique from the SSI method and the state variable derivative approach from deadbeat current control methods. The goal is to alleviate the single-sampling-period delay linked with DBCC. The newly suggested approach effectively reduces the delay from one sampling period to a quarter of a sampling period ($\frac{1}{4}$), all without the need for an anti-aliasing filter. This enhancement not only minimizes the delay but also broadens the controller bandwidth, enhancing the system's ability to handle fluctuations in parameters.

1.7 Outline of thesis

This thesis is composed of eight chapters and is based on a set of articles published in peer-review journals. These articles presented theoretical and simulation results that addressed each objective set in this thesis.

Chapter 1: The background of the study, the problem statement, the aim of this research work, and the research objectives, scope, and contribution are presented.

Chapter 2: This chapter gives a concise review of research works related to time-delay compensation in grid-connected inverter application.

Chapter 3: The methodology used in the research is presented. This includes the step-by-step procedure for achieving the set objectives.

Chapter 4: A comprehensive review and analysis of the relevant literature regarding time-delay compensation for a grid-connected inverter are presented.

Chapter 5: The design and simulation of five prominent deadbeat current controllers for grid-connected inverter application with the best response time and robustness again parameter variations are presented to address the first objective.

Chapter 6: The analysis of the proposed quadruple-sampling state-variable-derivative deadbeat current control method with time delay is presented to address the second objective.

Chapter 7: A comparison between the performances of the proposed controller and the PI current controller is presented to address the third objective.

Chapter 8: The conclusion and recommendations for future works are presented in this chapter.

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APPENDIX E

LIST OF PUBLICATIONS

1. **G. Elhassan**, S. A. Zulkifli, E. Pathan, M. H. Khan, and R. Jackson, "A Comprehensive Review on Time-Delay Compensation Techniques for Grid-Connected Inverters," IET Renewable Power Generation, vol. 15, no. 2, pp. 251–266, Feb. 2021, doi: 10.1049/rpg2.12033.
2. **G. Elhassan**, S. A. Zulkifli1, S. Z. Iliya, H. Bevrani4, M. Kabir1, R. Jackson1,M. H. Khan1, and M. Ahmed, "Deadbeat Current Control in Grid-Connected Inverters: A Comprehensive Discussion," IEEE Access, vol. 10, pp. 3990–4014, 2022, doi: 10.1109/ACCESS.2021.3138789.
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APPENDIX F

VITA

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